i960® HA/HD/HT Superscalar Microprocessors

Overview

The Highest Performance Yet For Embedded Computing Applications

The embedded market is experiencing major changes due to increased demand from consumers for quick delivery of large amounts of information. The information is provided in printed documents, over enterprise networks, and through telecommunication equipment. As the information increases in volume and complexity, the equipment used to transmit it must be upgraded accordingly. To keep up with market needs, designers are discovering they will soon need higher performance processors than those currently available for the embedded market. Anticipating this, Intel has been developing a new processor series based on the i960® RISC architecture to meet these needs.

Many designers have recognized the advantages of the i960 microprocessor family, resulting in over 2000 design wins to date and its position as the #1 selling RISC processor in 1992 and 1993[1]. The new series from this established architecture is the i960 Hx processor, consisting of three versions of processors that offer varying levels of superscalar performance. Several customers were interviewed, and hundreds of inputs were noted, before defining the features found on the i960 Hx processor. A summary of the features is listed in Table 1 and can be seen in the block diagram illustrated in Figure 1. In addition to customer input, proprietary simulation tools were used to select the optimal size for on-chip memory. The result is a processor series that expands the performance levels available to the embedded market, while keeping the total system cost stable.

The i960 Hx processor series will triple the performance available from the i960 architecture. The processors target embedded control tasks that require fast movement of large amounts of data. Anticipated applications include enterprise networking devices, non-impact printers, intelligent I/O, and telecommunications equipment. The i960 Hx processors are differentiated by the core speed. The i960 HA processor

	i960® HA Processor	i960® HD Processor	i960® HT Processor
C-Series Compatible Bus	x	x	x
C-Series Compatible Interrupt Controller	x	x	x
8-Kbyte Data Cache	x	x	x
3.3 Volt Operation	x	x	x
Speed Tripled Core			x
ICE	x	x	x
Two Integrated Timers	x	x	x
Maximum Internal Clock (MHz)	40	66	75

Table 1: i960® Hx Microprocessor

[1] Source: DataQuest 1993

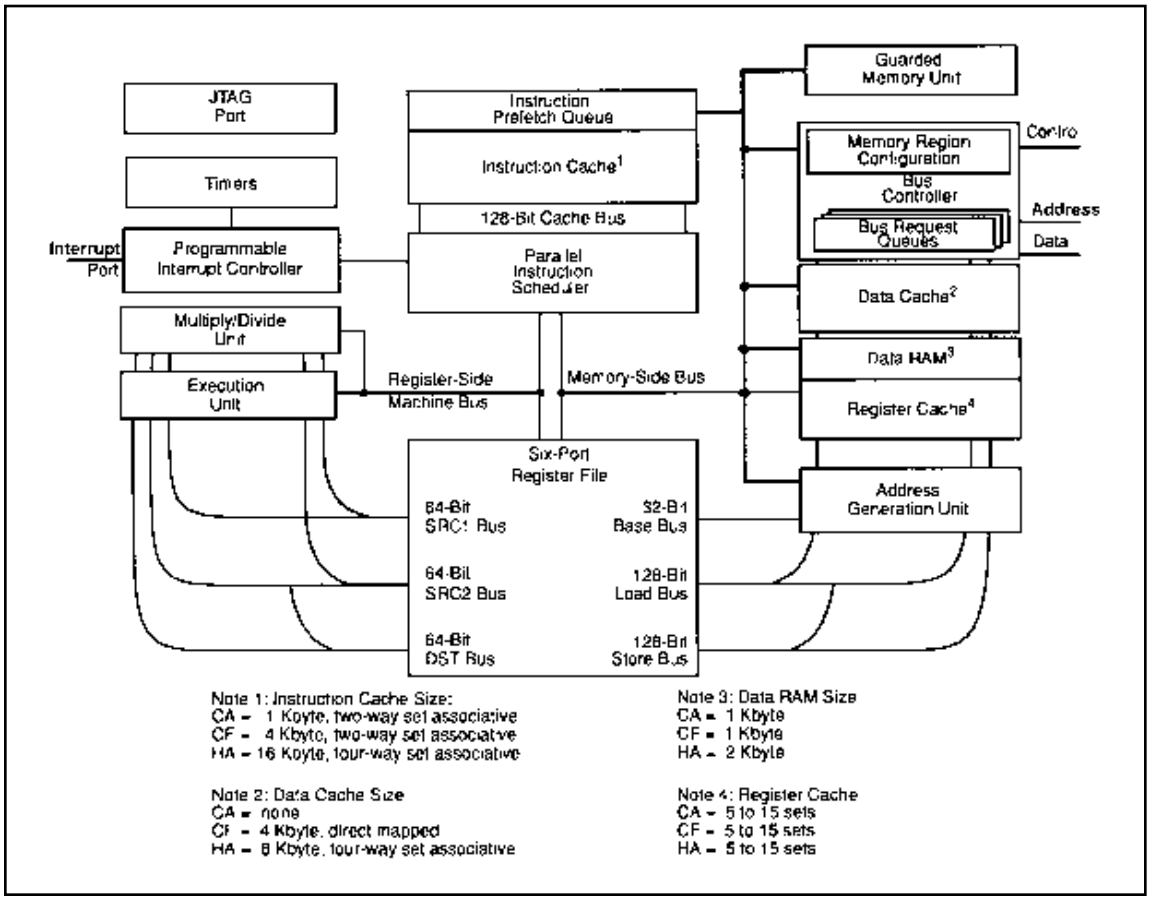

Figure 1: Intel's i960® Hx Microprocessor Block Diagram

core speed is equal to that of the external bus speed, the i960 HD processor core speed is twice that of the external bus speed, and the i960 HT processor core speed is three times the external bus speed. All three versions are 100% pin compatible, enabling quick moves to new price/performance points. The advantage of the i960 Hx processors to designers can be divided into five separate segments:

1) Performance

2) Ease of Design

3) State-of-the-Art Testability

4) Room to Grow

5) Total System Cost Reduction

Performance

The i960 Hx processors are able to provide performance levels unequaled in the embedded market because of the design of the fast superscalar core and the relationship of the core to the on-chip memory. The processor core is capable of maintaining an execution rate of two instructions per core clock. This translates to six instructions per bus clock for the clock-tripled i960 HT processor. The clock multiplier enables designers to develop systems with slower speed, less costly memory configurations. The ability to keep system cost low with a simple design is very useful to those sensitive to cost who still require high performance.

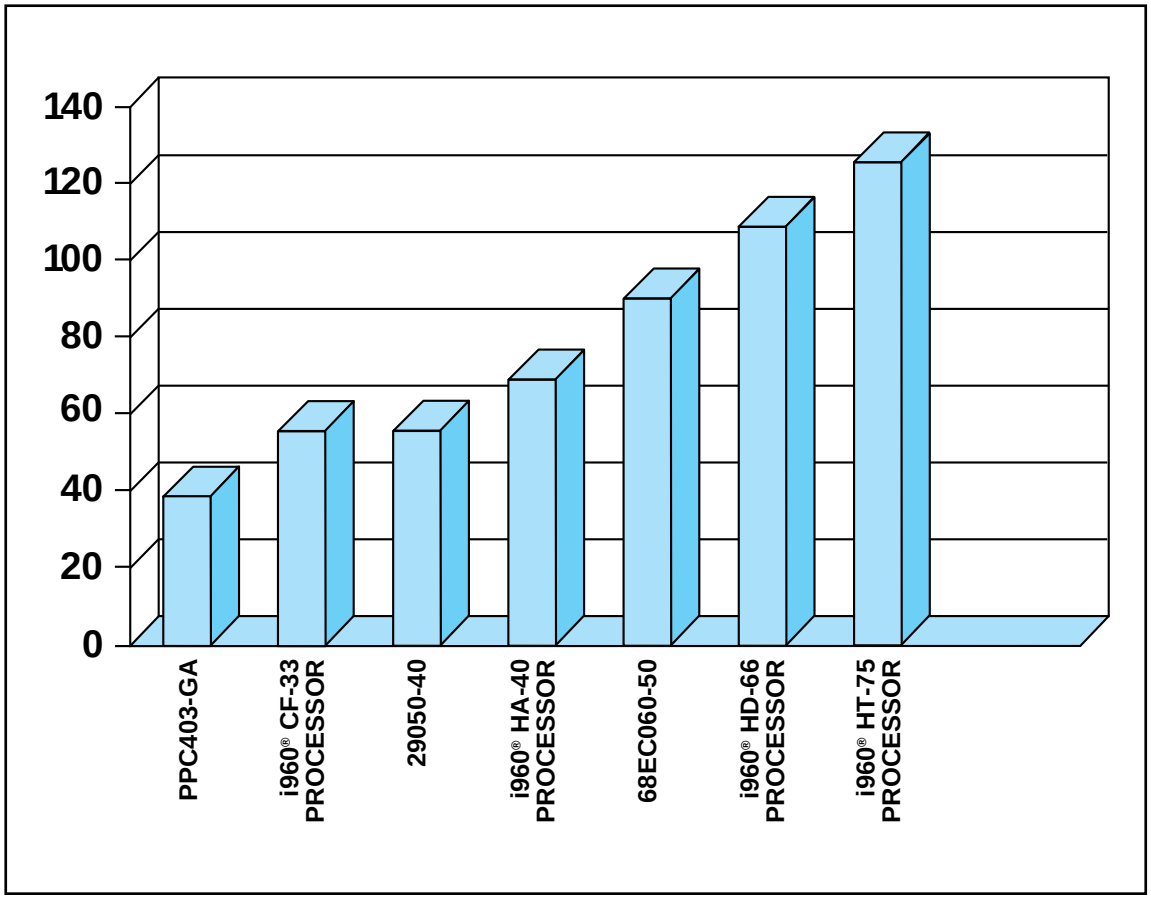

Figure 2: Relative Performance

Since all three versions of the i960 Hx processor series are 100% compatible, a single 25-MHz design can be used for the i960 HA-25, the i960 HD-50, and the i960 HT-75 processors. For comparison purposes, Figure 2 compares the number of VAX MIPS for several processors. It is clear that the i960 HD and i960 HT processors performance levels are substantially higher than the other processors listed, providing up to 125 VAX MIPS. When total system cost is included in the comparison, the i960 Hx processors look even better.

The core performance was further enhanced with the addition of new instructions. For example, compare instructions were added to allow compares for bytes and short-words without requiring shifts to mask unwanted bits. Simulation results suggest that these additional instructions could increase performance by 10 to 20%. Conditional instructions (for adds and subtracts) were also added. These conditional instructions can be used to reduce the number of branches in a code. This decreases the size of the code and improves the ability of the processor to use look-ahead logic by lengthening the basic and dynamic block lengths. Finally, a byte-swap instruction was added that changes the data-type from big endian to little endian, or vice-versa.

Unsurpassed Support of Unaligned Accesses

A significant improvement made with the i960 Hx processor is how it handles unaligned accesses. Most existing processors fault on unaligned accesses, forcing microcode to properly handle the access. Using microcode naturally takes execution time away from the core processor, negatively impacting performance. The i960 Hx processors have been designed to handle such accesses directly in hardware, eliminating the fault and the delay in handling the request. The response time is now up to 50% faster than those of native big endian processors.

Enhanced On-Chip Memory Keeps Processor Fed

A fast core processor serves little purpose unless it is constantly supplied with code and data. The i960 Hx processors have been designed to keep the processor fed, even when operating at a speed triple that of the external system. One of the major features that allows this is the enhancements made to the on-chip memory. Proprietary simulation tools were used to select the characteristics for the caches and data RAM. The programmable register cache allows up to 15 sets of 16 local registers each on-chip, for fast response to nested Calls and Returns. The programmer can determine how many register sets are reserved in the on-chip register cache for both normal routines and high priority interrupts. In this way, the embedded designer can optimize the configuration of the processor to match the behavior of the application program. For example, five register sets can be reserved to handle high priority interrupts so that they are always immediately available rather than waiting to allocate space on the "stack." This results in a guaranteed minimum interrupt latency, which is very useful in embedded applications.

The instruction cache has been designed to increase performance with both an increased depth of 16-Kbytes, four-way set-associative, and the ability to lock 4-Kbyte sections. In many cases, a designer can boost overall system performance dramatically if a certain critical piece of code can be locked into the cache. Programmers will often choose to lock interrupt handlers in the cache to minimize interrupt response times. The instruction cache can also be disabled to assist in evaluation of new code.

The i960 Hx processors provide an 8-Kbyte four-way set-associative data cache. The inclusion of a data cache is a significant performance enhancement for applications that keep data in slow speed memory. When required data is read from the cache, reads to the external bus are avoided, freeing up the bus for use by external agents such as Ethernet and Token Ring controllers. For use in multi-processor environments, the data cache can be invalidated completely, by region, or by individual address.

The i960 Hx processors also have 2 Kbyte of on-chip data RAM. This provides zero wait-state memory storage for data variables and interrupt vectors. Unlike data cache, variables can never be pushed out of the data RAM. The compilers use the RAM for storage of critical variables, resulting in fast and deterministic access to data.

Fast Response With On-Chip Interrupt Controller

The interrupt controller is very similar to the controller found on the i960 Cx processors. It provides a flexible, low-latency method for requesting interrupts. Interrupts are used very often in embedded applications and the interrupt controller has been designed to provide fast response times with a flexible environment. The controller supports one non-maskable interrupt, two timer interrupts and three modes: dedicated, expanded, and mixed. When the interrupt controller detects an active signal, the priority is compared to posted interrupts, independent of the core. If the priority is higher than those posted, the vector of the associated interrupt is located by the processor, and the interrupt is serviced. Otherwise, the interrupt is posted with no impact to

the core processor. The i960 Hx processors also improve interrupt performance through other techniques:

1) The processor core determines the address of the first instruction of the interrupt service routine from the priority vector. The processor allows caching of the interrupt vector addresses that point to the addresses of the first executable instruction. Reserved for this purpose are the first 64-bytes of on-chip data RAM. Storing these vectors in the on-chip RAM provides much faster response time.

2) To reduce the time necessary for the processor to fetch the first instruction to be executed, the i960 Hx processors can permanently lock critical sections of code, such as interrupt handlers in the instruction cache. This results in faster and more deterministic interrupt response time.

Ease of Design

The embedded market requires both low system costs and excellent performance. This apparent conflict has been resolved with the i960 Hx processors. The i960 Hx processors will offer core clock speeds of 25, 33, 40, 50, 66, and 75 MHz. A hardware designer will be able to develop a system built around a 25 MHz bus, and use either the i960 HA 25-, i960 HD 50-, or i960 HT 75-MHz processors. This flexibility allows a designer to choose from any number of combinations to meet the price/performance requirements of the application.

Adding to the flexibility of the processor is the ability to define separate physical and logical regions of memory. The physical memory is divided into 16 regions of 256 Mbytes each. The characteristics of each region are programmed into the 16 different PMCON registers. Some of the characteristics include burst support, parity, variable bus widths, and wait-states. This simplifies implementation of different memory types in an application. For example, one region could be 8-bit ROM for initialization, another region for 2 wait-state DRAM, and a third region for zero wait-state SRAM. The logical memory can be split into up to 16 regions of programmable size. The characteristics stored in the LMCON registers identify if the regions are cacheable and if it is big or little endian.

To assist in software evaluation, a guarded memory unit (GMU) has been integrated into the i960 Hx processors. The GMU is useful for those programmers who would like to store clean code in regions where the code cannot be manipulated. The GMU provides two levels of security to code generated by the programmer. The two levels are “protection” and “detection”. Two regions of memory can be designated as “protected”. The GMU will not allow accesses to code in these two regions; it will also generate a fault when such an access is attempted. Six more regions can be designated for “detection”. The GMU will allow access to these regions, but will detect the access and generate a fault signaling that the access has occurred.

Finally, embedded applications often require low power to keep down cooling costs. The i960 Hx processors operate at 3.3 Volts, but can support 5.0 I/Os. Also the i960 Hx processors include a Halt instruction which will put the processor into a reduced power mode, requiring 10% of the typical power.

State-of-the-Art Testability

The i960 Hx processors have been designed for easy manufacturability, both in terms of design and validation. The increasing size of the on-chip caches naturally results in a reduced number of external bus cycles, making it difficult to identify the true software execution path. The i960 HX processors integrate on-chip hardware breakpoint registers to simplify the development process. These registers consist of six instruction and six data breakpoints. These registers work with debuggers such as Intel’s DB-960 and

GDB-960. To further assist investigation of the execution of a program, the i960 Hx processor series support in-circuit emulators (ICE™). The technology allows the processor to execute at 99.5 percent of the normal execution rate with the ICE operating in the system. This provides true real-time debugging capability with full visibility into the processor. The i960 processor family is supported by the well known Solutions960® program, with more than 200 tools available from 73 vendors. To assist with hardware testing, the i960 Hx processors provide several methods of testing. BIST (built-in self-test) is an internal self-test which ensures confidence level in the processor before executing any system diagnostics. The Bus Confidence Test checks the external bus by reading eight words from the initialization boot record and performing a checksum on the words. The processors also support JTAG (IEEE 1149.1) for on-chip test logic.

Room to Grow

The ability to quickly proliferate products at new price/performance points is very important to successful manufacturers. The i960 Hx processors enable customers to quickly modify products to meet new market needs thanks to upward binary code compatibility and a wide variety of pin-compatible products. For this reason, knowledge in one processor will make the move to new processors extremely easy. The commercial versions of the entire i960 microprocessor family is illustrated in Figure 3. To further simplify the upgrade path, the PGA versions of the i960 Hx processors have to been designed to have a pin-out very similar to the i960 CA and i960 CF processors. Following the recommendations provided by Intel, a designer can develop one board which will accept any of the i960 Cx or i960 Hx processors in the same PGA socket. This creates the opportunity to get a jump on evaluating a design before the i960 Hx processors are available, or even to create one board which can be used to meet several different price points with a simple switch of the CPU.

The future holds even higher performance from the i960 architecture. Intel invests hundreds of millions of dollars each year into research and development leading to faster processors being manufactured more efficiently. As the i960 processor family takes advantage of this investment, expected enhancements include clock-quadrupling, processing speeds over 100 MHz, and even larger caches. Intel has already started defining the follow-on generation to the i960 Hx and Jx processors. The result is that a customer who selects the i960 architecture can relax knowing that an upgrade path exists for the future.

Total System Cost Reduction

When evaluating which processor is right for you, it is important to consider several factors. This brochure briefly discusses the features of the i960 Hx processors. The i960 Hx processor series has been developed to reduce your total system cost by enabling low speed memory to be used with a high speed processor. The development tools available with the processor will result in a fast turn from conception to production, and bring in revenue faster than possible with processors with less established development tools. Further reducing the total cost, the i960 Hx processor is priced right for the cost sensitive embedded market.

Please contact your Intel sales representative for the latest pricing information and more detailed documentation on the i960 Hx processors.

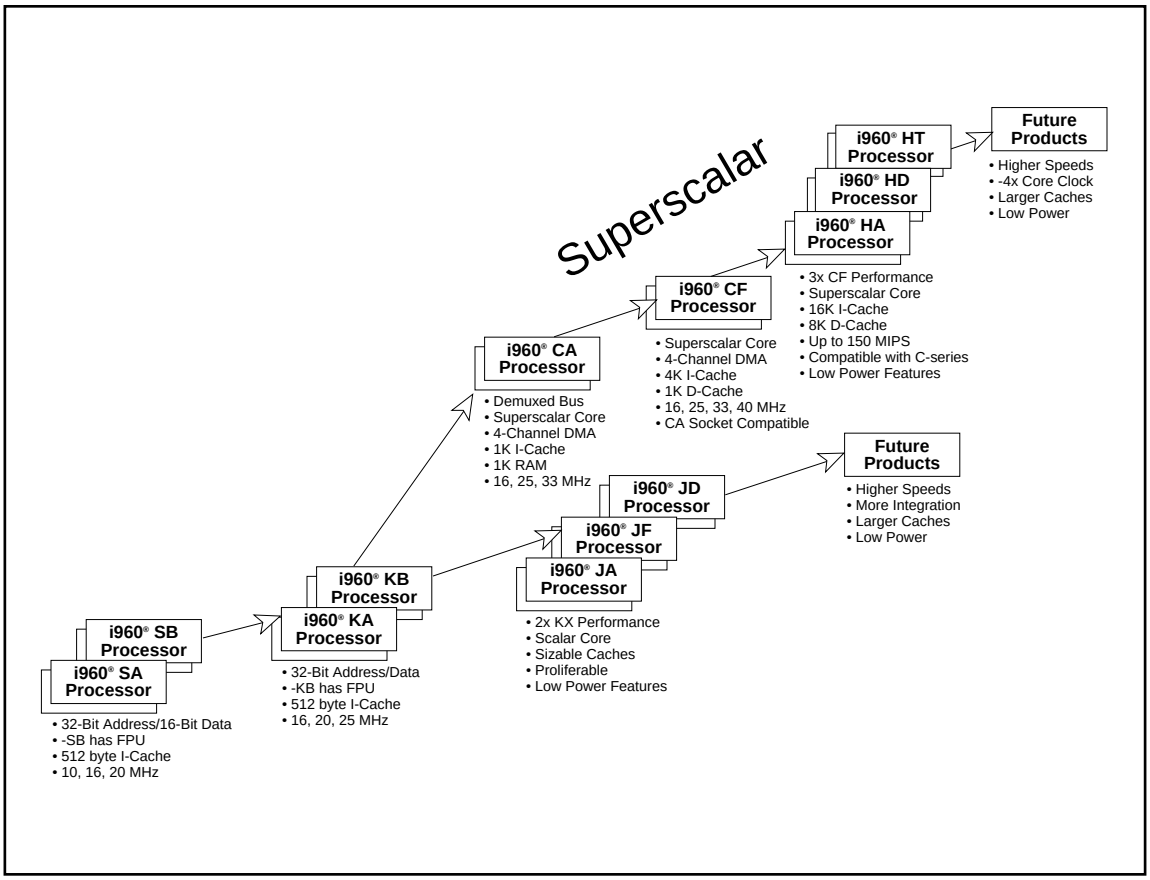

Figure 3: Room to Grow: i960® Microprocessor Roadmap

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Product and Sales Information	Intel product information, sales office and distributor phone numbers	**800-628-8686**
Literature Department	To order Intel product literature.	**800-548-4725**
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